CHARACTERIZATION OF EPITAXIAL SILICON FOR MOS VLSI IC BY DEEP LEVEL TRANSIENT SPECTROSCOPY AND MINORITY CARRIER LIFETIME MEASUREMENTS

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The effect of silicon source contamination on the properties of epitaxial layers was studied by DLTS technique and generation lifetime measurements. The influence of substrate etching procedure on the generation lifetime is also shown.

Introduction

Epitaxial silicon is widely used as starting material for small geometry CMOS devices. However, during the epitaxial growth a variety of native defects and impurities are introduced into the layers. When located in the active region of devices, these point defects, particularly transition metal impurities, have strong detrimental effect on the device performance. So, for the quality assessment of epitaxial silicon for MOS VLSI integrated circuits it is necessary to control the type and concentration of point defects as well as the minority carrier lifetime.

In this paper we present the results of characterization of epitaxial silicon by deep level transient spectroscopy (DLTS) and measurements of the generation carrier lifetime in MOS structures.

Experimental procedure

The p+ and n+ starting substrates for epitaxy were 100mm diameter CZ wafers with <111> orientation. The p+ wafers were boron doped with the resistivity in the range of 0.01-0.02 Ωcm. The n+ wafers were antimony doped with the resistivity in the range of 0.008-0.018 Ωcm.
The wafers were prepared by standard lapping, wet etching and polishing processing. In the case of the n⁺ substrate two different types of chemical etchant have been used:

- acid solution, consisted of HNO₃, HF and CH₃COOH,
- alkaline solution, consisted of KOH and stabilizers.

All the other mechano-chemical treatments, including final cleaning were identical for all substrates.

The epitaxial layers were deposited in a rf heated Gemini 1 reactor of vertical type with rotated pancake-like graphite susceptor. An in-situ HCl etching at 1180°C was used to remove about 1μm of the silicon layer prior to the deposition. The epitaxial deposition was performed at 1120°C with the growth rate of 1μm/min.

Two silicon sources were used for epitaxial growth: SiCl₄ and SiHCl₃. As dopants 25vpm B₂H₆ in H₂ was used for the p-type layers and 25 vpm PH₃ in H₂ for the n-type layers.

In the test processes, performed without intentional doping, the resistivity of layers grown from SiCl₄ was 180 Ωcm and 800 Ωcm in the case of using SiHCl₃.

The layer thickness was measured by means of a standard infrared reflection spectrophotometer. The resistivity was determined by spreading resistance method. The majority carrier concentration profiling by C-V method with Hg probe was also made.

For the carrier generation lifetime measurement the gate silicon oxide of 1000 thickness was deposited on the layer surface. The electrical contact to the oxide was made by means of Hg probe of 1mm diameter. The value of carrier lifetime in the obtained MOS structures was calculated by Zerbst method.

The measurements were performed using computer-controlled CSM/16 System with Hg probe (Materials Development Corp.).

DLTS measurements were performed on Schottky diodes fabricated by Au evaporation onto the surface of epitaxial layers. Measurements were carried out by a standard DLS 81 equipment. Temperature scans were performed for various rate windows (2 - 2000 s⁻¹) with increasing temperature in the range of 80-300K and the
temperature dependence of the carrier emission rate $e_n=f(T)$ was determined. The reverse bias was -10V and filling pulse amplitude was equal to 9V. The energy levels were determined from Arrhenius plots $\ln(e_n/T^2)\text{vs }1/T$. The deep centre concentration $N_T$ was calculated from the well-known relation [1]:

$$N_T = 2\Delta C(N_D-N_A)/C_{st}$$

where $\Delta C$ is the DLTS output, $C_{st}$ is the quiescent capacitance of the reverse-biased diode and $N_D-N_A$ is the majority carrier concentration.

**Experimental results and discussion**

The main purpose of our studies was to show how the uncontrolled impurities affect the quality of the epitaxial layers.

In the first experiment the epitaxial layer of 10 $\mu$m thickness and 10 $\Omega \text{cm}$ resistivity were deposited from two silicon sources of different test resistivity. According to the results presented in Table 1, in both types of epistructures ($n/n^+$ and $p/p^+$) the source contamination influence on the carrier generation lifetime is clearly seen.

**Table 1. Dependence of $\tau_g$ on silicon source used for epitaxy.**

<table>
<thead>
<tr>
<th>Structure</th>
<th>Silicon source</th>
<th>Gen. lifetime $\tau_g[\mu s]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n/n^+$</td>
<td>$\text{SiCl}_4$ - test resistivity 180 $\Omega \text{cm}$</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td>$\text{SiHCl}_3$ - test resistivity 800 $\Omega \text{cm}$</td>
<td>115</td>
</tr>
<tr>
<td>$p/p^+$</td>
<td>$\text{SiCl}_4$ - as above</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>$\text{SiHCl}_3$ - as above</td>
<td>400</td>
</tr>
</tbody>
</table>

The DLTS spectra for epitaxial layers deposited from $\text{SiCl}_4$ and $\text{SiHCl}_3$ are shown in Fig.1 and Fig.2 respectively. The Arrhenius plots for deep-level defects detected in the epitaxial layers are presented in Fig. 3.
Fig. 1. DLTS spectrum for epitaxial layers deposited from SiCl₄.

Fig. 2. DLTS spectrum for epitaxial layers deposited from SiHCl₃.
Fig. 3. Arrhenius plots for deep-level defects detected in the epitaxial layers grown from SiCl$_4$ and SiHCl$_3$.

Table 2. Parameters of deep traps detected in epitaxial layers grown from SiHCl$_3$ and SiCl$_4$.

<table>
<thead>
<tr>
<th>Trap</th>
<th>$T_1$</th>
<th>$T_2$</th>
<th>$T_3$</th>
<th>$T_4$</th>
<th>$T_5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_a$ [eV]</td>
<td>-</td>
<td>0.27</td>
<td>0.41</td>
<td>0.56</td>
<td>-</td>
</tr>
<tr>
<td>$\sigma_a$ [cm$^{-3}$]</td>
<td>-</td>
<td>$1.0 \times 10^{-13}$</td>
<td>$2.0 \times 10^{-12}$</td>
<td>$4.0 \times 10^{-12}$</td>
<td>-</td>
</tr>
<tr>
<td>$N_T$ [cm$^{-3}$]</td>
<td>-</td>
<td>$2.8 \times 10^{13}$</td>
<td>$8.0 \times 10^{10}$</td>
<td>$7.0 \times 10^{11}$</td>
<td>-</td>
</tr>
</tbody>
</table>

SiCl$_4$, $N_D-N_A = 9.6 \times 10^{13}$ [cm$^{-3}$]

SiHCl$_3$, $N_D-N_A = 3 \times 10^{12}$ [cm$^{-3}$]
The results of the silicon source characterization obtained from DLTS measurements are presented in Table 2.

According to the data presented in Table 2 the concentration of deep traps in the epitaxial layers deposited from SiHCl₃ is by three orders of magnitude lower than in that obtained from SiCl₄. These traps are likely to be attributed to transition metal impurities [2].

In the second experiment the epitaxial layers were grown on the n⁺ substrates prepared by alkaline etching as well as by acid etching. The influence of the residual alkaline ions in the n type epitaxial layers on the carrier lifetime is shown in the Table 3. As alkaline ions result in decreasing carrier lifetime, substrates for the high epitaxy standard should be etched in the acid solution.

Table 3. Dependence of $\tau_g$ on substrate chemical etching.

<table>
<thead>
<tr>
<th>Layer parameters</th>
<th>Generation lifetime, $\tau_g$ $[\mu s]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness [μm]</td>
<td>Resistivity [Ωcm]</td>
</tr>
<tr>
<td>9.5</td>
<td>3.5</td>
</tr>
<tr>
<td>18.5</td>
<td>47.0</td>
</tr>
</tbody>
</table>

Conclusions

The carrier generation lifetime measurements on MOS epitaxial structures can be used as a criteria of the quality of epitaxial layers.

The DLTS measurements give additional useful information on the properties and concentration of deep traps. So, DLTS is also powerful tool for quality characterization of materials used in the epitaxy processes.

According to the obtained data, uncontrolled impurities in epitaxial layers are mainly introduced from the source of silicon used for epitaxy. Substrate etching in alkaline solution have to be avoided in the MOS VLSI production.
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References

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